DIY Electronics

Southern Cross II

8031 Single Board Computer

Hardware Manual

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Introduction

The Southern Cross II single board computer is based around the 8032/52 8-bit microcontroller. Adding a power supply and connecting to any PC capable of running an 8051 cross-assembler enables the user to implement an 8031 software development system. Programming in BASIC is also possible using one of the 8052-BASIC chips currently available. If your board is fitted with one of these BASIC chips then switching from one software environment to the other is simply a matter of inserting or removing a link.

The Southern Cross II, when used in conjunction with the MVS-31 debugging monitor, implements a complete 8031-based assembly language software development system. The extra resources provided by an 8032/52 over an 8031,(extra timer and an additional 128 bytes of internal RAM memory), together with an independent external UART allows the user complete access to all the 8031's internal ports and timers. Software debugging tools such as breakpoints, watchpoints and single stepping are provided by the MVS-31 monitor program. Refer to the "MVS-31 User's manual" for further details.

Getting Started

Running in 8031 mode

Insert the MVS-31 monitor EPROM into socket IC4 and ensure that jumper JP2 is set to the correct EPROM type. An 8032/52 microcontroller chip must be used in position IC1.

1. Insert a link on jumper JP1.
2. Move switch SW2 to the OFF position.
3. Connect a 9 - 12 volt DC plug pack via power connector J7.
4. Connect the supplied serial cable to connector **J5 ("HOST" port)**. Connect a terminal or PC (running terminal emulation software) to the D25 connector on the cable. Configure the terminal or PC serial port to 8 data bits, 1 stop bit and no parity. The baud rate should be set to 1200, 2400, 4800, 9600 or 19200 bps.
5. Turn on the power via switch SW3. LED D2 should light.
6. Press the Carriage Return (Enter↵) key to trigger the MVS-31 automatic baud rate detection. A sign on banner will appear followed by a " > " prompt. Commands may now be entered.

Running in BASIC mode

This mode requires an 8052-BASIC microcontroller chip in position IC1. A 27256 EPROM is also necessary in position IC4 if BASIC programs are to be saved into EPROM. Ensure that jumper JP2 is set to the correct EPROM type.

1. Remove the link from jumper JP1.
2. Move switch SW2 to the OFF position.
3. Connect a 9 - 12 volt DC plug pack via power connector J7.
4. Connect the supplied serial cable to connector **J6 ("USER" port)**. Connect a terminal or PC (running terminal emulation software) to the D25 connector on the cable. Configure the terminal or PC serial port to 8 data bits, 1 stop bit and no parity. The baud rate should be set to 1200, 2400, 4800, 9600 or 19200 bps.
5. Turn on the power via switch SW3. LED D2 should light.
6. Press the space bar to trigger the BASIC-52 automatic baud rate detection. A sign on message will appear followed by a "READY" prompt. Commands may now be entered.

Please read the section on "BASIC-52 Programming" before attempting to save any programs into EPROM.

EPROM types

The Southern Cross II can use three different EPROM types, 8K (2764), 16K (27128) and 32K (27256). The EPROM type is selected by setting jumper JP2 to the correct position as marked on the circuit board.

Note that in order to save BASIC programs in EPROM, a 27256 EPROM must be used.

Southern Cross II Memory Map

This manual does not aim to provide a detailed explanation of the architecture of the 8051 family of microcontrollers. However a short description is necessary so that the memory decoding scheme can be explained and understood.

The 8051 family of microcontrollers implement the Harvard memory architecture. This means that these devices have **separate** address spaces for Program and Data memory, each up to 64K in size. Internal circuitry in the microcontroller accesses the correct memory based on the instruction being executed.

As well as having separate Program and Data spaces, these microcontrollers also have internal and external Program and Data memory. The 8051/52 series of microcontrollers can have up to 8K of internal program memory. Thus any program address in the range 0000h to 1FFFh is directed to internal Program memory. Any other program address is directed externally. It is possible to direct all program access externally by disabling internal program memory. This is done by connecting the /EA pin to ground. The 8031/32 series have no internal program memory so all program access must be directed externally. The microcontrollers running BASIC are 8052 series chips with the BASIC interpreter stored in internal program memory.

Program memory can only be read, not written to, The /PSEN signal is used as a read strobe for any **external** program memory. Data memory occupies a separate address space from Program memory. The /RD and /WR signals are used to access **external** Data memory as needed. Only Data memory can be written to and programs can only run from Program memory!

It is possible to combine all or part of the Program and Data memory into one address space. This is done by logically ORing the /PSEN and /RD signals with the decoded memory range required and using the resultant output as a read strobe. Combining Program and Data memory is necessary on the Southern Cross II so that users can download and run programs.

The Southern Cross II provides 16K of RAM memory that is accessible as both Program and Data memory. This is the area of memory where user programs are downloaded into and executed from. The other 16K of RAM is accessible as Data memory only.

The EPROM can be an 8K, 16K or 32K type. The EPROM address space is split, with 16K located at 0000h and the other 16K located at 8000h. The 16K block at 8000h is used to store BASIC programs when the Southern Cross II is used as a BASIC computer! Refer to the "BASIC-52 Programming" reference manuals for more information.

All external I/O devices such as the SPI and PPI chips are located in external data memory. Remember that only data memory can be written to!

Figure 1 gives an overall picture of the Southern Cross II memory map.

Memory and I/O decoding is provided via two programmable logic devices (GALs). Using GALs for address mapping adds great flexibility to the circuit design as well as significantly reducing chip count. Other memory and I/O address mapping schemes are possible by re-programming the GALs.
Contact DIY Electronics for further information.

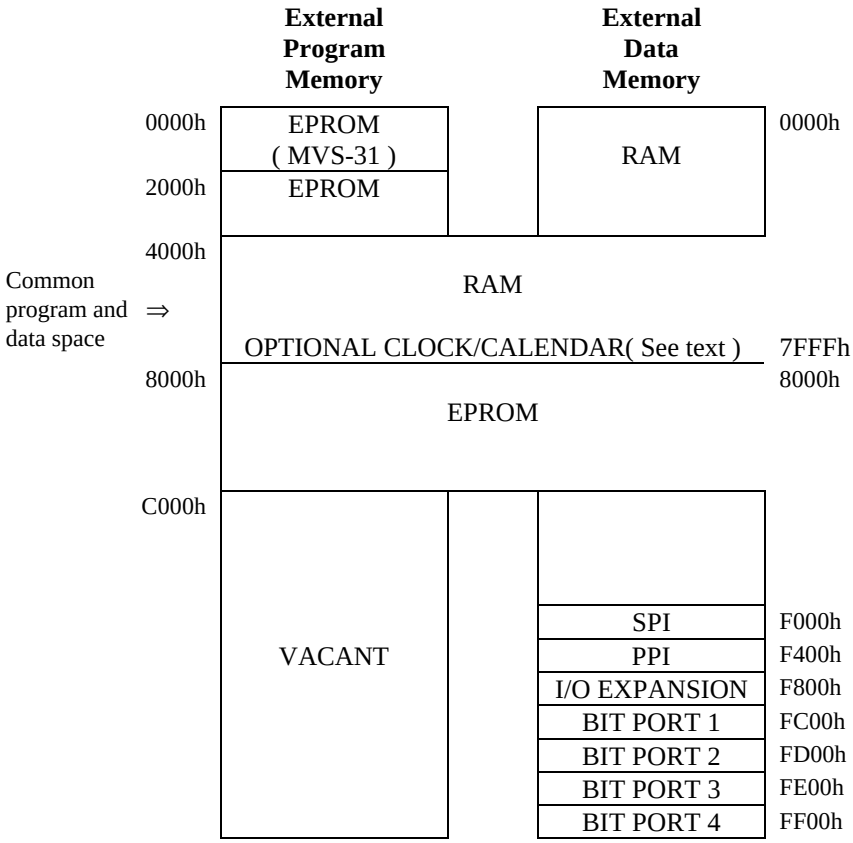


Fig 1

Serial Ports

These are implemented as simple "3-wire" interfaces, using just TxD, RxD and GND. The modem control lines "CTS, DSR and DCD" are held at the RS-232 "ON" level and do not provide any hardware handshaking. No software handshaking protocol is used either.

The Southern Cross II has two serial ports.

1. Uses the internal serial port of the 8032/52 chip and is referred to as the "USER" port. Connection is via the 10-pin header labelled J6.
2. Uses an external SC2691 UART chip from Philips Components and is referred to as the "HOST" port. Connection is via the 10-pin header labelled J5

The RS-232 signals are brought out to standard D9 connectors by using a 10-way flat ribbon cable. One end is terminated with a 10-pin IDC plug and the other end with a crimp-style female D9 connector. By connecting pin 1 on the 10-pin plug with pin 1 on the D9 connectors, the signals will be in the correct positions to allow a "straight-through" connection to a D9-type PC COM port.

RS-232 Interface - J5, J6

Signal	J5, J6 pin	D9 pin
TxD	3	2
RxD	5	3
CTS	6	8
DSR	2	6
GND	9	5
DCD	1	1

Parallel I/O Ports

A number of parallel I/O ports are provided. Some are "static" in operation, meaning that any data written to the port is latched. The other ports are "dynamic" in nature. These ports do not latch data written to them. Output data is only valid while the port is being addressed. These ports are referred to as "bit ports".

8031 I/O ports - J1

The 8051 family of microcontrollers have four inbuilt 8-bit parallel ports, labelled P0-3. Two of these ports, P0 and P2, are used as address/data busses when external program and data memory access is required. This is the mode in which the Southern Cross II operates. Port bits P3.6 and P3.7 are used as /RD and /WR signals and therefore are not available for use as I/O lines. This leaves 13 I/O lines available for use, all of port 1 and bits 0-5 of port 3. Note that port bits P3.0 - P3.5 all have secondary functions eg. P3.0 and P3.1 are the Rx and Tx lines for the 8031 serial port.

These 13 I/O lines are brought out to a 16-pin header labelled J1.

J1 pin	Signal	J1 pin	Signal
1	P1.0	2	P1.1
3	P1.2	4	P1.3
5	P1.4	6	P1.5
7	P1.6	8	P1.7
9	P3.0 / RxD	10	P3.1 / TxD
11	P3.2 / INT0	12	P3.3 / INT1
13	P3.4 / T0	14	P3.5 / T1
15	GND	16	GND

Port bits P1.3, P1.4 ans P1.5 also have a secondary function. They are connected via switch SW2 to the memory decoder GAL, IC9, and used by the 8052-BASIC chips as EPROM programming control pins. These pins are only needed by BASIC-52 when programs are to be saved into EPROM. Refer to the section on "BASIC-52 Programming" for further details.

8255 I/O Ports - J2

Three 8-bit parallel ports are implemented using the 8255 Programmable Peripheral Interface (PPI) chip (IC6). This chip is mapped in external data memory at address F400h. These 24 I/O lines are brought out to a 26-pin header labelled J2.

J2 pin	Signal	J2 pin	Signal
1	PA0	2	PA1
3	PA2	4	PA3
5	PA4	6	PA5
7	PA6	8	PA7
9	PB0	10	PB1
11	PB2	12	PB3
13	PB4	14	PB5
15	PB6	16	PB7
17	PC0	18	PC1
19	PC2	20	PC3
21	PC4	22	PC5
23	PC6	24	PC7
25	GND	26	GND

Bit Ports - J4

As mentioned previously, these are "dynamic" not static ports. With referrence to sheet 2 of the schematic diagram, the 8 I/O lines are actually driven by the data bus (BAD0 - 7). The ports are formed by decoding a 256 byte memory block and using the resulting output as an active low strobe, similar to the chip enable signals for the EPROM and RAM chips. These 4 bit ports are mapped in external data memory at the following address locations:

Bit port 1	FC00h
Bit port 2	FD00h
Bit port 3	FE00h
Bit port 4	FF00h

Although each port is mapped into a 256 byte block, it is only one address "wide". Therefore bit port 1 can be accessed at address FC00h, FC01h, FC02h ... etc right through to FCFFh. These ports are both input and output ports, depending on the instruction used to access them.

These ports are pin for pin compatible to the CN1 port on the Z80 based "Southern Cross" computer, also available from DIY Electronics. It is provided on the Southern Cross II to take advantage of a number of add-on boards already available for the "Southern Cross" computer.

The bit ports are brought out to a 16-pin header labelled J4.

J4 pin	Signal	J4 pin	Signal
1	+5V	2	/RESET
3	/BIT PORT 1	4	/BIT PORT 2
5	/BIT PORT 3	6	/BIT PORT 4
7	GND	8	GND
9	BAD4	10	BAD3
11	BAD5	12	BAD2
13	BAD6	14	BAD1
15	BAD7	16	BAD0

I/O Expansion Interface - J3

A maximum of 256 bytes of I/O expansion is available via connector J3. This interface allows for further devices to be connected to the microcontroller. The interface is mapped in external data memory beginning at address location F800h.

J3 pin	Signal	J3 pin	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	AD0	10	AD1
11	AD2	12	AD3
13	AD4	14	AD5
15	AD6	16	AD7
17	/RD	18	/WR
19	RESET	20	ALE
21	/IOEXP	22	
23	+5V	24	+5V
25	GND	26	GND

Signals preceeded by " / " are active low, all other signals are active high.

The signal " /IOEXP " is the block decode signal for the expansion interface and should be used in conjunction with address lines A0-A7 to provide further address decoding.

Address lines A0-A7 have already been de-mulitplexed on the Southern Cross II board ie. they are actually address lines. This allows devices with separate address and data lines to be connected to the expansion interface directly. For those devices with a multiplexed address/data bus use signals AD0-AD7 and ALE.

Clock/Calendar

An optional clock/calendar device is available for the Southern Cross II, a Dallas Semiconductor DS1216C Intelligent Socket. Access to this clock/calendar is provided in the MVS-31 debugging monitor.

The DS1216C contains an internal lithium battery. This keeps the clock going during power down and also makes the CMOS RAM non-volatile ie. no loss of data when power to the Southern Cross II is removed.

Battery life is over 10 years. No circuit modifications are necessary to use the DS1216C, just plug it in between the RAM chip and the IC socket (or solder directly to the PCB if purchased with the Southern Cross II kit).

BASIC-52 Programming

As mentioned, the Southern Cross II board is capable of being programmed in BASIC. A number of suppliers, such as Intel and Micromint Inc., have available an 8052 microcontroller with a BASIC interpreter programmed into the chip's internal EPROM. The Southern Cross II needs one of these chips installed as IC1 in order run the BASIC-52 language.

BASIC-52 has the ability to store its programs into an external memory device such as EPROM. Programming EPROMs requires a voltage level of between 12.5 and 25 volts (depending on the EPROM). The Southern Cross II generates this programming voltage using a DC-DC converter chip, IC12.

The Southern Cross II is designed to use a 27256 EPROM for storing BASIC programs. These EPROMs require a programming voltage of 12.5 volts. Before attempting to save any programs in EPROM, the programming voltage must be set to this level. This is done by measuring the voltage on test pin TP1 and adjusting trimpot VR1 for 12.5 volts. This procedure is only required once. However it is worth checking this voltage periodically or whenever any problems occur with saving programs to EPROM.

The Southern Cross II only uses 27256 EPROMs for saving BASIC programs. Remove the MVS-31 monitor EPROM and install a 27256 type in its place. The MVS-31 monitor can reside on the same 27256 EPROM used to save BASIC programs. The monitor would reside in the bottom 8K starting at address 0000h whereas BASIC programs are saved at address locations 8000h upwards, which is in the upper 16K of the EPROM. The memory decoder GAL, IC9, splits the EPROM into two halves, with one half starting at 0000h and the other half starting at 8000h. Remember to set jumper JP2 to the correct EPROM type. A number of BASIC-52 programming and startup options are also available. Refer to the BASIC-52 reference manual for further details.

BASIC-52 uses port bits P1.3, P1,4 and P1.5 as EPROM programming control lines. The function of these lines is:

P1.3	ALE Disable
P1.4	Program pulse width
P1.5	Enable program voltage

These signals are not connected directly to the EPROM or associated programming circuitry. Instead they are connected via switch SW2 and the memory decoder GAL, IC9. When the GAL detects a low on its pin 5, it uses these port bits to control the output signals " /ROM_CE, SYS_ALE and /VPP_CONT ". Moving SW2 to the " ON " position connects the port bits to the GAL and pulls pin 5 low, ready for EPROM programming.

These port bits can also be used as general purpose I/O lines and are brought out on connector J1. These pins MUST be isolated from any external voltage levels. This would be the case if any of these pins were inputs

being "driven" from a device connected to J1. Therefore, it is advisable before saving programs to EPROM to disconnect any device from J1.

To summarize, the following steps must be carried out before issuing a BASIC-52 programming command.

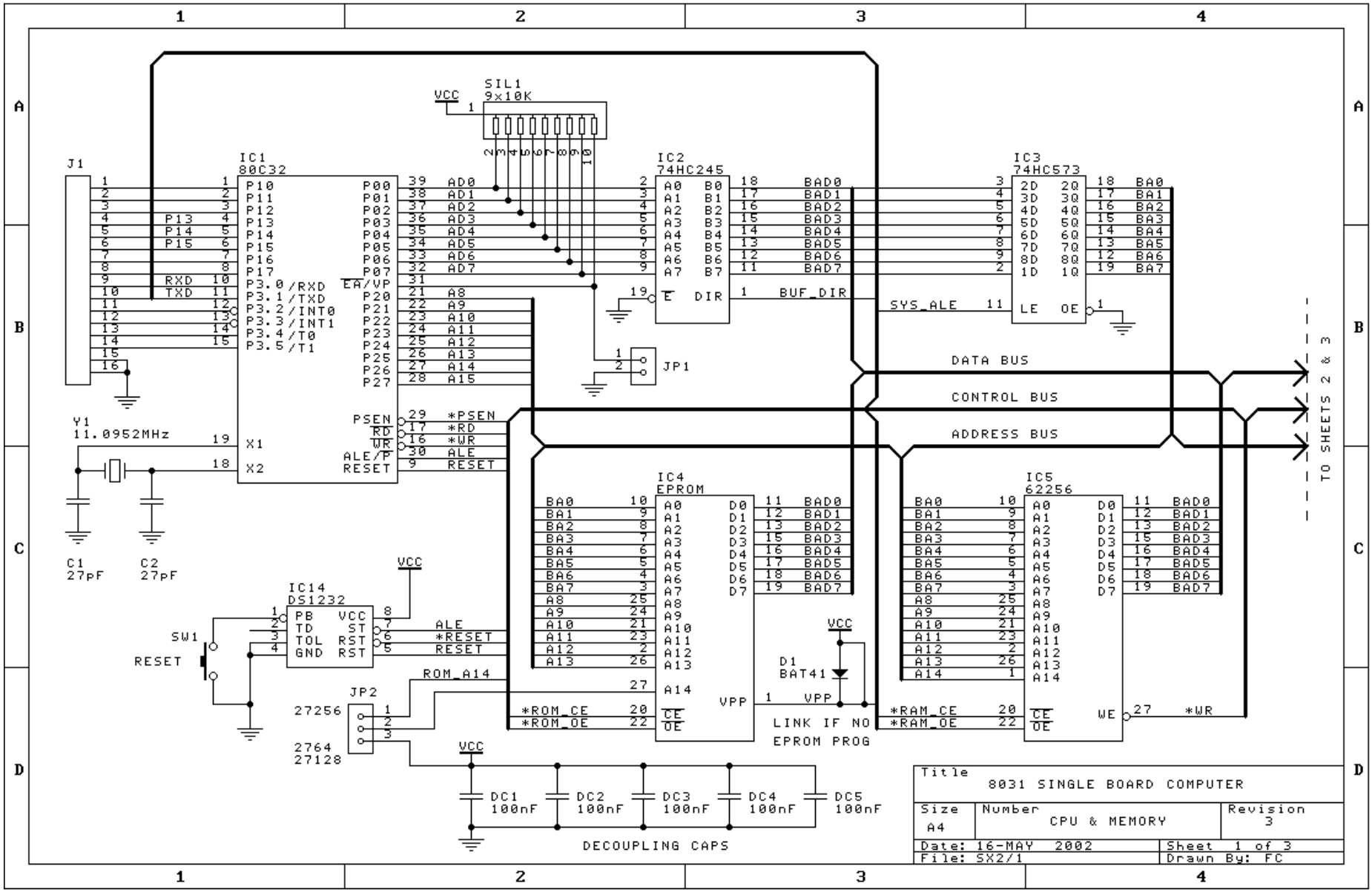
1. Disconnect any device attached to connector J1.
2. Move switch SW2 to the " ON " position.

Whilst the MVS-31 monitor program and BASIC programs can be stored on the same 27256 EPROM it is advisable to use two separate EPROMs. If you wish to keep them together then make a copy of the MVS-31 EPROM and use the copy instead. The MVS-31 binary file is on the disk supplied with the Southern Cross II computer.

References

The hardware & software for the Southern Cross 2 were developed by Frank Crivelli for DIY Electronics. Frank can be contacted at **frank@ozitronics.com**

The following web sites contain 80xx code & material
http://www.lvr.com
http://livewire.ee.latrobe.edu/~sjm
http://cera2.com/gatox805.htm
http://www.atmel.com


J1
IC1
80C32
P10
P11
P12
P13
P14
P15
P16
P17
P3.0/RXD
P3.1/TXD
P3.2/INT0
P3.3/INT1
P3.4/T0
P3.5/T1
P00
P01
P02
P03
P04
P05
P06
P07
EA/VP
P20
P21
P22
P23
P24
P25
P26
P27
PSEN
RD
WR
ALE/P
RESET
X1
X2
SIL1
9x10K
VCC
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
A8
A9
A10
A11
A12
A13
A14
A15
*PSEN
*RD
*WR
ALE
RESET
IC2
74HC245
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
E
DIR
BAD0
BAD1
BAD2
BAD3
BAD4
BAD5
BAD6
BAD7
BUF_DIR
JP1
IC3
74HC573
2D
3D
4D
5D
6D
7D
8D
1D
2Q
3Q
4Q
5Q
6Q
7Q
8Q
1Q
LE
OE
SYS_ALE
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
DATA BUS
CONTROL BUS
ADDRESS BUS
TO SHEETS 2 & 3
Y1
11.0952MHz
C1
27pF
C2
27pF
IC14
DS1232
PB
TD
TOL
GND
VCC
ST
RST
RST
SW1
RESET
ALE
*RESET
RESET
IC4
EPROM
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
VPP
CE
OE
*ROM_CE
*ROM_OE
ROM_A14
JP2
27256
2764
27128
D1
BAT41
LINK IF NO
EPROM PROG
IC5
62256
*RAM_CE
*RAM_OE
WE
*WR
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100nF
DC2
100nF
DC3
100nF
DC4
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DC5
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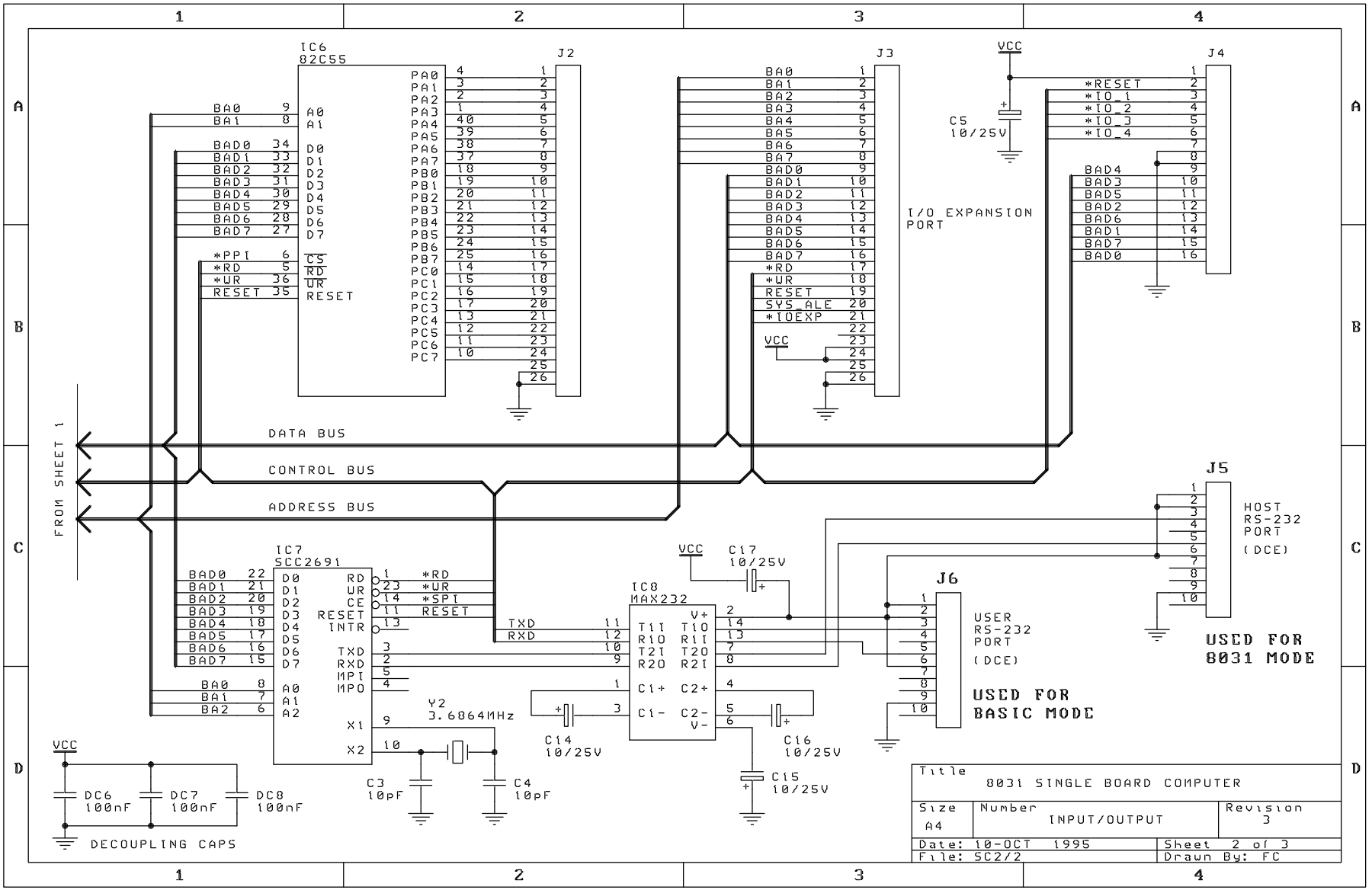
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BAD7
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*WR
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PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
A0
A1
D0
D1
D2
D3
D4
D5
D6
D7
CS
RD
WR
RESET
DATA BUS
CONTROL BUS
ADDRESS BUS
FROM SHEET 1
IC7
SCC2691
D0
D1
D2
D3
D4
D5
D6
D7
RD
WR
CE
RESET
INTR
TXD
RXD
MPI
MPO
X1
X2
*RD
*WR
*SPI
RESET
Y2
3.6864MHz
C3
10pF
C4
10pF
IC8
MAX232
T1I
R1O
T2I
R2O
T1O
R1I
T2O
R2I
V+
V-
C1+
C1-
C2+
C2-
C14
10/25V
C15
10/25V
C16
10/25V
C17
10/25V
J5
HOST
RS-232
PORT
(DCE)
J6
USER
RS-232
PORT
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DC8
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Revision
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Sheet 2 of 3
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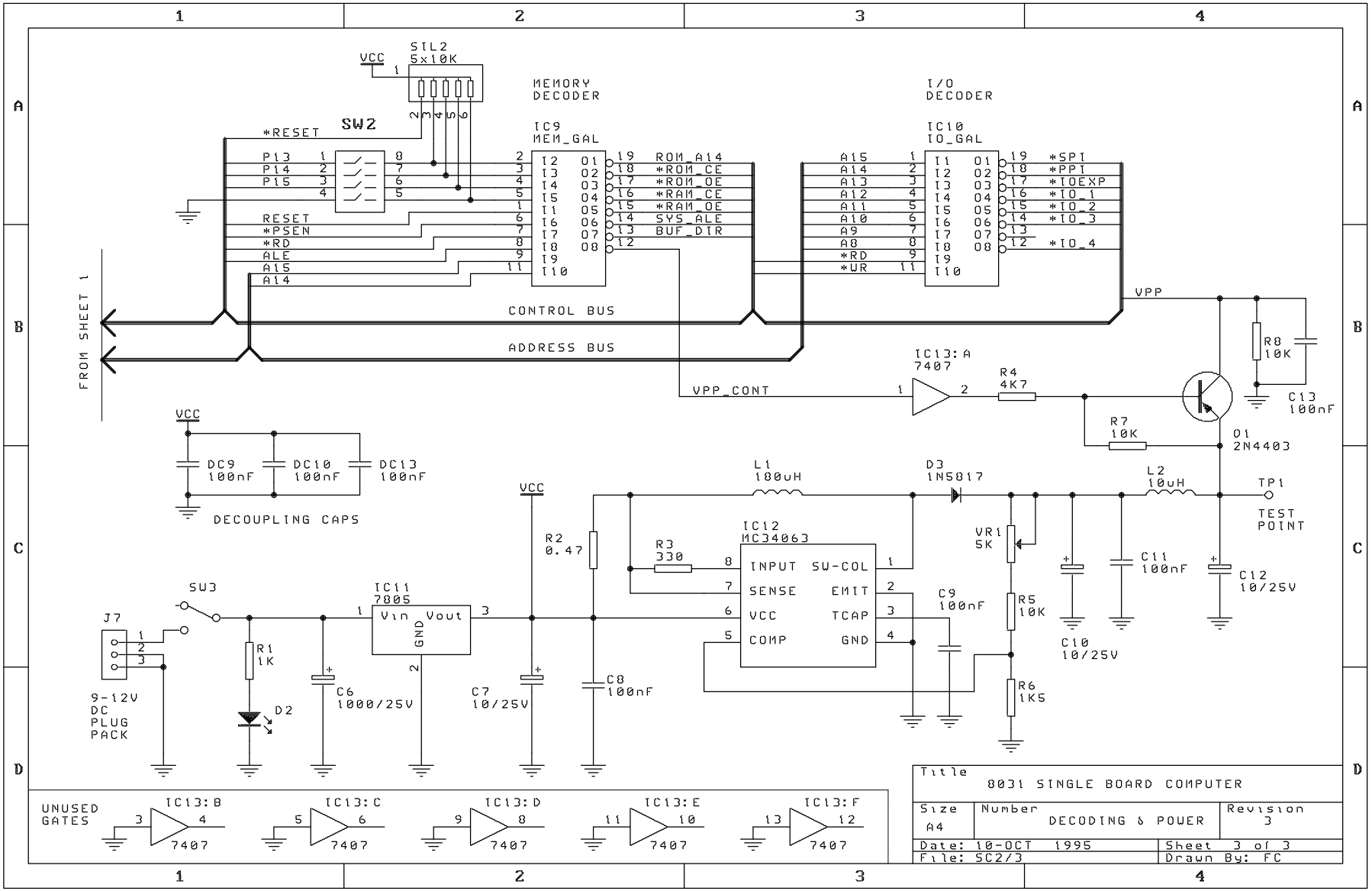
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*IOEXP
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*IO_2
*IO_3
*IO_4
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ADDRESS BUS
VPP
VPP_CONT
IC13:A
7407
R4
4K7
R8
10K
C13
100nF
R7
10K
Q1
2N4403
DC9
100nF
DC10
100nF
DC13
100nF
DECOUPLING CAPS
L1
180uH
D3
1N5817
L2
10uH
TP1
TEST
POINT
R2
0.47
R3
330
IC12
MC34063
INPUT
SENSE
VCC
COMP
SW-COL
EMIT
TCAP
GND
VR1
5K
C9
100nF
R5
10K
R6
1K5
C10
10/25V
C11
100nF
C12
10/25V
SW3
J7
9-12V
DC
PLUG
PACK
R1
1K
D2
IC11
7805
Vin
Vout
GND
C6
1000/25V
C7
10/25V
C8
100nF
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GATES
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IC13:C
IC13:D
IC13:E
IC13:F
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8031 SINGLE BOARD COMPUTER
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Number
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Revision
3
Date: 10-OCT 1995
Sheet 3 of 3
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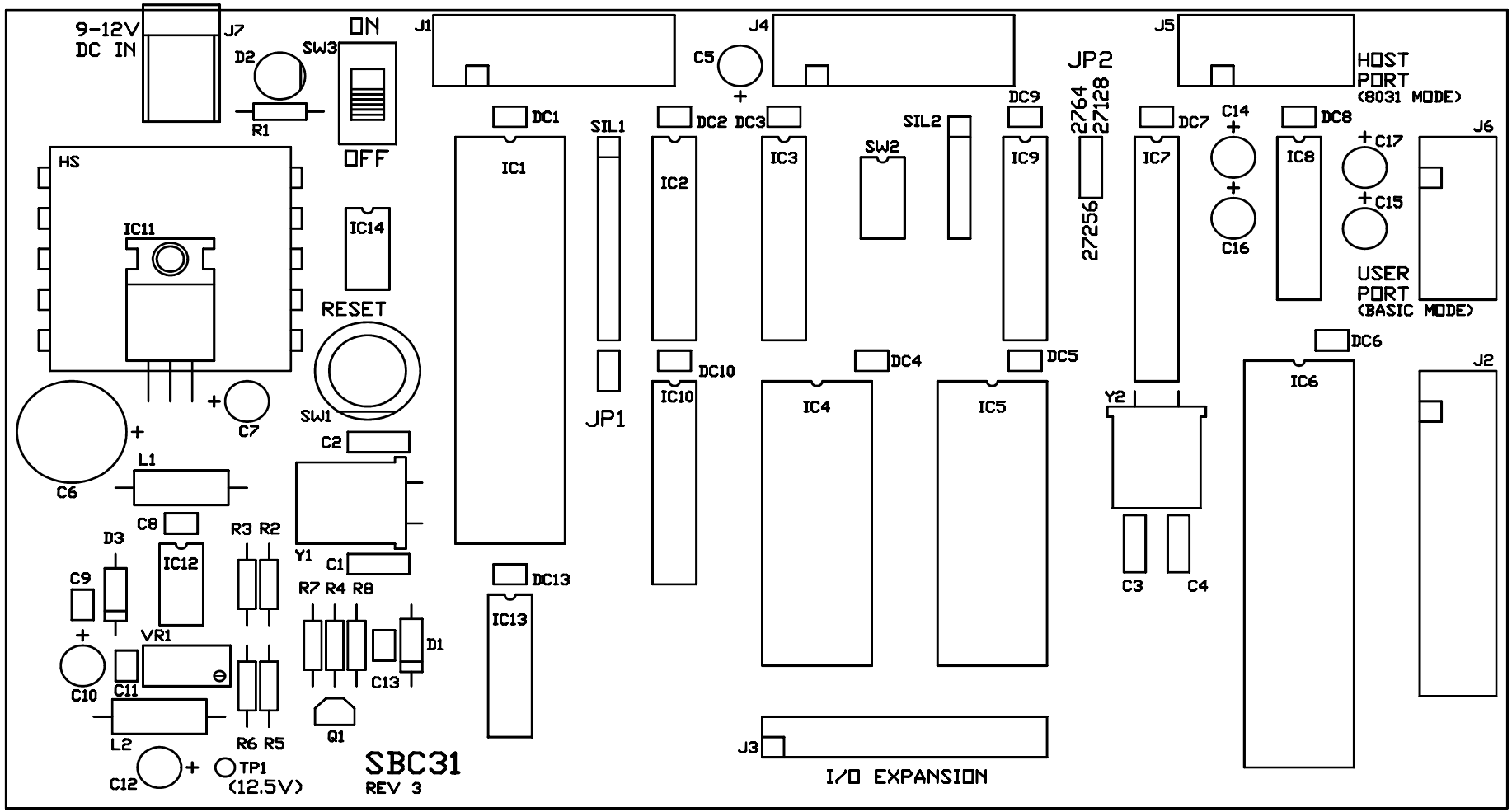
Drawn By: FC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J7
D2
R1
SW3
ON
OFF
J1
J4
C5
JP2
2764
27128
27256
J5
HOST
PORT
(8031 MODE)
HS
IC11
IC14
RESET
SW1
C7
C6
L1
C2
Y1
C1
C8
D3
IC12
R3 R2
C9
R7 R4 R8
VR1
C10
C11
C13
D1
L2
R6 R5
Q1
C12
TP1
(12.5V)
SBC31
REV 3
DC1
IC1
SIL1
JP1
DC2
IC2
DC3
IC3
SW2
SIL2
DC9
IC9
DC7
IC7
C14
C16
DC8
IC8
C17
C15
J6
USER
PORT
(BASIC MODE)
DC10
IC10
DC4
IC4
DC5
IC5
Y2
C3
C4
DC6
IC6
J2
DC13
IC13
J3
I/O EXPANSION